

# ARTAFLEX

## AWM24xxL Register Details

### Register Descriptions

All registers are read and writable, except where noted. Registers may be written to or read from either individually or in sequential groups. A single-byte read or write reads or writes from the addressed register. Incrementing burst read and write is a sequence that begins with an address, and then reads or writes to/from each register in address order for as long as clocking continues. It is possible to repeatedly read (poll) a single register using a non-incrementing burst read.

**Table 9-1. Register Map Summary**

Address	Mnemonic	b7	b6	b5	b4	b3	b2	b1	b0	Default <sup>(1)</sup>	Access <sup>(1)</sup>	
0x00	CHANNEL_ADR	Not Used	Channel							-1001000	-bbbbbbb	
0x01	TX_LENGTH_ADR	TX Length								00000000	bbbbbbbb	
0x02	TX_CTRL_ADR	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN	00000011	bbbbbbbb	
0x03	TX_CFG_ADR	Not Used	Not Used	DATA CODE LENGTH	DATA MODE		PA SETTING			--000101	--bbbbbb	
0x04	TX_IRQ_STATUS_ADR	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQ	10111000	rrrrrrrr	
0x05	RX_CTRL_ADR	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN	00000111	bbbbbbbb	
0x06	RX_CFG_ADR	AGC EN	LNA	ATT	HILO	FASTTURN EN	Not Used	RXOW EN	VLD EN	10010-10	bbbb-bb	
0x07	RX_IRQ_STATUS_ADR	RXOW IRQ	SOFDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ	00000000	rrrrrrrr	
0x08	RX_STATUS_ADR	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode		00001---	rrrrrrrr	
0x09	RX_COUNT_ADR	RX Count								00000000	rrrrrrrr	
0x0A	RX_LENGTH_ADR	RX Length								00000000	rrrrrrrr	
0x0B	PWR_CTRL_ADR	PMU EN	LVIRQ EN	PMU SEN	Not Used	LVI TH		PMU OUTV		10100000	bbb-bbbb	
0x0C	XTAL_CTRL_ADR	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ			000--100	bbb--bbb	
0x0D	IO_CFG_ADR	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO	00000000	bbbbbbbb	
0x0E	GPIO_CTRL_ADR	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP	0000----	bbbbrrrr	
0x0F	XACT_CFG_ADR	ACK EN	Not Used	FRC END	END STATE			ACK TO		1-000000	b-bbbbb	
0x10	FRAMING_CFG_ADR	SOP EN	SOP LEN	LEN EN	SOP TH					10100101	bbbbbbbb	
0x11	DATA32_THOLD_ADR	Not Used	Not Used	Not Used	Not Used	TH32					----0100	----bbbb
0x12	DATA64_THOLD_ADR	Not Used	Not Used	Not Used	TH64					---01010	---bbbb	
0x13	RSSI_ADR	SOP	Not Used	LNA	RSSI					0-100000	r-rrrrrr	
0x14	EOP_CTRL_ADR	HEN	HINT				EOP				10100100	bbbbbbbb
0x15	CRC_SEED_LSB_ADR	CRC SEED LSB								00000000	bbbbbbbb	
0x16	CRC_SEED_MSB_ADR	CRC SEED MSB								00000000	bbbbbbbb	
0x17	TX_CRC_LSB_ADR	CRC LSB								-----	rrrrrrrr	
0x18	TX_CRC_MSB_ADR	CRC MSB								-----	rrrrrrrr	
0x19	RX_CRC_LSB_ADR	CRC LSB								11111111	rrrrrrrr	
0x1A	RX_CRC_MSB_ADR	CRC MSB								11111111	rrrrrrrr	
0x1B	TX_OFFSET_LSB_ADR	STRIM LSB								00000000	bbbbbbbb	
0x1C	TX_OFFSET_MSB_ADR	Not Used	Not Used	Not Used	Not Used	STRIM MSB					----0000	----bbbb
0x1D	MODE_OVERRIDE_ADR	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST	00000-0	wwww-w	
0x1E	RX_OVERRIDE_ADR	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used	0000000-	bbbbbbbb-	
0x1F	TX_OVERRIDE_ADR	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV	00000000	bbbbbbbb	
0x27	CLK_OVERRIDE_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwww	
0x28	CLK_EN_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwww	
0x29	RX_ABORT_ADR	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD	00000000	wwwwwww	
0x32	AUTO_CAL_TIME_ADR	AUTO_CAL_TIME_MAX								00000011	wwwwwww	
0x35	AUTO_CAL_OFFSET_ADR	AUTO_CAL_OFFSET_MINUS_4								00000000	wwwwwww	
0x39	ANALOG_CTRL_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ALL SLOW	00000000	wwwwwww	
Register Files												
0x20	TX_BUFFER_ADR	TX Buffer File								-----	wwwwwww	
0x21	RX_BUFFER_ADR	RX Buffer File								-----	rrrrrrrr	
0x22	SOP_CODE_ADR	SOP Code File								Note 2	bbbbbbbb	
0x23	DATA_CODE_ADR	Data Code File								Note 3	bbbbbbbb	
0x24	PREAMBLE_ADR	Preamble File								Note 4	bbbbbbbb	
0x25	MFG_ID_ADR	MFG ID File								NA	rrrrrrrr	

#### Notes:

1. b = read/write, r = read only, w = write only, - = not used, default value is undefined.
2. SOP\_CODE\_ADR default = 0x17FF9E213690C782.
3. DATA\_CODE\_ADR default = 0x02F9939702FA5CE3012BF1DB0132BE6F.
4. PREAMBLE\_ADR default = 0x333302.

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## AWM24xxL Register Details

Mnemonic	CHANNEL_ADR						Address	0x00
Bit	7	6	5	4	3	2	1	0
Default	-	1	0	0	1	0	0	0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used	Channel						
<div>Bits 6:0</div> <div>This field selects the channel. 0x00 sets 2400 MHz; 0x62 sets 2498 MHz. Values above 0x62 are not valid. The default channel is a fast channel above the frequency typically used in non-overlapping WiFi systems. Any write to this register will impact the time it takes the synthesizer to settle.</div> <div>fast (100-μs) - 0 3 6 9 12 15 18 21 24 27 30 33 36 39 42 45 48 51 54 57 60 63 66 69 72 96</div> <div>medium (180-μs) - 2 4 8 10 14 16 20 22 26 28 32 34 38 40 44 46 50 52 56 58 62 64 68 70 74 76 78 80 82 84 86 88 90 92 94</div> <div>slow (270-μs) - 1 5 7 11 13 17 19 23 25 29 31 35 37 41 43 47 49 53 55 59 61 65 67 71 73 75 77 79 81 83 85 87 89 91 93 95 97</div> <div>Usable channels subject to regulation.</div>								

Mnemonic	TX_LENGTH_ADR			Address				0x01
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TX Length							
Bits 7:0	<p>This register sets the length of the packet to be transmitted. A length of zero is valid, and will transmit a packet with SOP, length and CRC16 fields (if enabled), but no data field. Packet lengths of more than 16 bytes will require that some data bytes be written after transmission of the packet has begun. Typically, length is updated prior to setting TX GO. The maximum packet length for all packets is 40 bytes except for framed 64-chip DDR where the maximum packet length is 16 bytes.</p> <p>Maximum packet length is limited by the delta between the transmitter and receiver crystals of 60-ppm or better.</p>							

Mnemonic	TX_CTRL_ADR			Address				0x02
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN
<p>Bit 7 Start Transmission. Setting this bit triggers the transmission of a packet. Writing a 0 to this flag has no effect. This bit is cleared automatically at the end of packet transmission. The transmit buffer may be loaded either before or after setting this bit. If data is loaded after setting this bit, the length of time available to load the buffer depends on the starting state (sleep, idle or synth), the length of the SOP code, the length of preamble, and the packet data rate. For example, if starting from idle mode on a fast channel in 8DR mode with 32 chip SOP codes the time available is 100 μs (synth start) + 32 μs (preamble) + 64 μs (SOP length) + 32 μs (length byte) = 228 μs. If there are no bytes in the TX buffer at the end of transmission of the length field, a TXBERR IRQ will occur.</p> <p>Bit 6 Clear TX Buffer. Writing a 1 to this register clears the transmit buffer. Writing a 0 to this bit has no effect. The previous packet may be retransmitted by setting TX GO and not setting this bit. A new transmit packet may be loaded and transmitted without setting this bit if TX GO is set after the new packet is loaded to the buffer. If the TX_BUFFER_ADR is to be loaded after the TX GO bit has been set, then this bit should be set before loading a new transmit packet to the buffer and before TX GO is set.</p> <p>Bit 5 Buffer Not Full Interrupt Enable. See TX_IRQ_STATUS_ADR for description.</p> <p>Bit 4 Buffer Half Empty Interrupt Enable. See TX_IRQ_STATUS_ADR for description.</p> <p>Bit 3 Buffer Empty Interrupt Enable. See TX_IRQ_STATUS_ADR for description.</p> <p>Bit 2 Buffer Error Interrupt Enable. See TX_IRQ_STATUS_ADR for description.</p> <p>Bit 1 Transmission Complete Interrupt Enable. See TX_IRQ_STATUS_ADR for description. TXC IRQEN and TXE IRQEN must be set together.</p> <p>Bit 0 Transmit Error Interrupt Enable. See TX_IRQ_STATUS_ADR for description. TXC IRQEN and TXE IRQEN must be set together.</p>								

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## AWM24xxL Register Details

Mnemonic	TX_CFG_ADR			Address				0x03
Bit	7	6	5	4	3	2	1	0
Default	-	-	0	0	0	1	0	1
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Data Code Length	Data Mode		PA Setting		
Bit 5	Data Code Length. This bit selects the length of the DATA_CODE_ADR code for the data portion of the packet. This bit is ignored when the data mode is set to GFSK. 1 = 64 chip codes. 0 = 32 chip codes.							
Bits 4:3	Data Mode. This field sets the data transmission mode. 00 = 1-Mbps GFSK. 01 = 8DR Mode. 10 = DDR Mode. 11 = SDR Mode. It is recommended that firmware sets the ALL_SLOW bit in register ANALOG_CTRL_ADR when using GFSK data rate mode.							
Bits 2:0	PA Setting. This field sets the transmit signal strength. 0 = -30 dBm, 1 = -25 dBm, 2 = -20 dBm, 3 = -15 dBm, 4 = -10 dBm, 5 = -5 dBm, 6 = 0 dBm, 7 = +4 dBm.							

Mnemonic	TX_IRQ_STATUS_ADR			Address				0x04
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	1	1	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Function	OS IRQ	LV IRQ	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQ
The state of all IRQ status bits is valid regardless of whether or not the IRQ is enabled. The IRQ output of the device is in its active state whenever one or more bits in this register is set and the corresponding IRQ enable bit is also set. Status bits are non-atomic (different flags may change value at different times in response to a single event). In particular, standard error handling is only effective if the premature termination of a transmission due to an exception does not leave the device in an inconsistent state.								
Bit 7	Oscillator Stable IRQ Status. This bit is set when the internal crystal oscillator has settled (synthesizer sequence starts).							
Bit 6	Low Voltage Interrupt Status. This bit is set when the voltage on V <sub>BAT</sub> is below the LVI threshold (see PWR_CTL_ADR). This interrupt is automatically disabled whenever the PMU is disabled. When enabled, this bit reflects the voltage on V <sub>BAT</sub> .							
Bit 5	Buffer Not Full Interrupt Status. This bit is set whenever there are 15 or fewer bytes remaining in the transmit buffer.							
Bit 4	Buffer Half Empty Interrupt Status. This bit is set whenever there are 8 or fewer bytes remaining in the transmit buffer.							
Bit 3	Buffer Empty Interrupt Status. This bit is set at any time that the transmit buffer is empty.							
Bit 2	Buffer Error Interrupt Status. This IRQ is triggered by either of two events: (1) When the transmit buffer (TX_BUFFER_ADR) is empty and the number of bytes remaining to be transmitted is greater than zero. (2) When a byte is written to the transmit buffer and the buffer is already full. This IRQ is cleared by setting bit TX CLR in TX_CTRL_ADR.							
Bit 1	Transmission Complete Interrupt Status. This IRQ is triggered when transmission is complete. If transaction mode is not enabled then this interrupt is triggered immediately after transmission of the last bit of the CRC16. If transaction mode is enabled, this interrupt is triggered at the end of a transaction. Reading this register clears this bit. TXC IRQ and TXE IRQ flags may change value at different times in response to a single event. If transaction mode is enabled and the first read of this register returns TXC IRQ=1 and TXE IRQ=0 then firmware must execute a second read to this register to determine if an error occurred by examining the status of TXE. There can be a case when this bit is not triggered when ACK EN = 1 and there is an error in transmission. If the first read of this register returns TXC IRQ = 1 and TXE IRQ = 1 then the firmware must not execute a second read to this register for a given transaction. If an ACK is received RXC IRQ and RXE IRQ may be asserted instead of TXC IRQ and TXE IRQ.							
Bit 0	Transmit Error Interrupt Status. This IRQ is triggered when there is an error in transmission. This interrupt is only applicable to transaction mode. It is triggered whenever no valid ACK packet is received within the ACK timeout period. Reading this register clears this bit.							

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## AWM24xxL Register Details

Mnemonic	RX_CTRL_ADR			Address				0x05
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN
Status bits are non-atomic (different flags may change value at different times in response to a single event).								
Bit 7	Start Receive. Setting this bit causes the device to transition to receive mode. If necessary, the crystal oscillator and synthesizer will start automatically after this bit is set. Firmware must never clear this bit. This bit must not be set until after it self clears. The recommended method to exit receive mode when an error has occurred is to force END STATE and then dummy read all RX_COUNT_ADR bytes from RX_BUFFER_ADR or poll RSSI_ADR.SOP (bit 7) until set. See XACT_CFG_ADR and RX_ABORT_ADR for description.							
Bit 6	Start of Packet Detect Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 5	Buffer Full Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 4	Buffer Half Empty Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 3	Buffer Not Empty Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 2	Buffer Error Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 1	Packet Reception Complete Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							
Bit 0	Receive Error Interrupt Enable. See RX_IRQ_STATUS_ADR for description.							

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## AWM24xxL Register Details

Mnemonic	RX_CFG_ADR			Address			0x06	
Bit	7	6	5	4	3	2	1	0
Default	1	0	0	1	0	-	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
Function	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN

Status bits are non-atomic (different flags may change value at different times in response to a single event).

Bit 7 Automatic Gain Control (AGC) Enable. When this bit is set, AGC is enabled, and the LNA is controlled by the AGC circuit. When this bit is cleared the LNA is controlled manually using the LNA bit. Typical applications will clear this bit during initialization. It is recommended that this bit be disabled and bit 6 (LNA) be enabled unless the device will be used in a system where it may receive data from a device using an external PA to transmit signals at >+4 dBm.

Bit 6 Low Noise Amplifier (LNA) Manual Control. When AGC EN (Bit 7) is cleared, this bit controls the state of the receiver LNA; when AGC EN is set, this bit has no effect. Setting this bit enables the LNA; clearing this bit disables the LNA. Device current in receive mode is slightly lower when the LNA is disabled. Typical applications will set this bit during initialization.

Bit 5 Receive Attenuator Enable. Setting this bit enables the receiver attenuator. The receiver attenuator may be used to de-sensitize the receiver so that only very strong signals may be received. This bit should only be set when the AGC EN is disabled and the LNA is manually disabled.

Bit 4 HILO. When FAST TURN EN is set, this bit is used to select whether the device will use the high frequency for the channel selected, or the low frequency. 1 = hi; 0 = lo. When FAST TURN EN is not enabled this also controls the highlow bit to the receiver and should be left at the default value of 1 for high side receive injection. Typical applications will clear this bit during initialization.

Bit 3 Fast Turn Mode Enable. When this bit is set, the HILO bit determines whether the device receives data transmitted 1MHz above the RX Synthesizer frequency or 1 MHz below the receiver synthesizer frequency. Use of this mode allows for very fast turn-around, because the same synthesizer frequency may be used for both transmit and receive, thus eliminating the synthesizer re-settling period between transmit and receive. Note that when this bit is set, and the HILO bit is cleared, received data bits are automatically inverted to compensate for the inversion of data received on the "image" frequency. Typical applications will set this bit during initialization.

Bit 1 Overwrite Enable. When this bit is set, if an SOP is detected while the receive buffer is not empty, then the existing contents of receive buffer are lost, and the new packet is loaded into the receive buffer. When this bit is set, the RXOW IRQ is enabled. If this bit is cleared, then the receive buffer may not be over-written by a new packet, and whenever the receive buffer is not empty SOP conditions are ignored, and it is not possible to receive data until the previously received packet has been completely read from the receive buffer.

Bit 0 Valid Flag Enable. When this bit is set, the receive buffer can store only 8 bytes of data. The other half of the buffer is used to store valid flags. See RX\_BUFFER\_ADR for more detail.

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## AWM24xxL Register Details

Mnemonic	RX_IRQ_STATUS_ADR			Address				0x07
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R	R	R	R	R	R	R
Function	RXOW IRQ	RSVD	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ
<p>The state of all IRQ Status bits is valid regardless of whether or not the IRQ is enabled. The IRQ output of the device is in its active state whenever one or more bits in this register is set and the corresponding IRQ enable bit is also set. Status bits are non-atomic (different flags may change value at different times in response to a single event). In particular, standard error handling is only effective if the premature termination of a transmission due to an exception does not leave the device in an inconsistent state.</p>								
Bit 7	Receive Overwrite Interrupt Status. This IRQ is triggered when the receive buffer is over-written by a packet being received before the previous packet has been read from the buffer. This bit is cleared by writing any value to this register. This condition is only possible when the RXOW EN bit in RX_CFG_ADR is set. This bit must be written "1" by firmware before the new packet may be read from the receive buffer.							
Bit 6	Reserved. Must not be set.							
Bit 5	Receive Buffer Full Interrupt Status. This bit is set whenever the receive buffer is full, and cleared otherwise.							
Bit 4	Receive Buffer Half Full Interrupt Status. This bit is set whenever there are 8 or more bytes remaining in the receive buffer. Firmware must read exactly eight bytes when reading RXB8 IRQ. It is possible, in rare cases, that the last byte of a packet may remain in the buffer even though the RXB1_IRQ flag has cleared. This can ONLY happen on the last byte of a packet and only if the packet data is being read out of the buffer while the packet is still being received. The flag is trustworthy under all other conditions, and for all bytes prior to the last. When using RXB1_IRQ and unloading the packet data during reception, the user should be sure to check the RX_COUNT_ADR value after the RXC/RXE is set and unload the last remaining byte if the number of bytes unloaded is less than the reported count, even though the RXB1_IRQ is not set							
Bit 3	Receive Buffer Not Empty Interrupt Status. This bit is set at any time that there are 1 or more bytes in the receive buffer., and cleared when the receive buffer is empty. RXB1 IRQ must not be set when RXB8 IRQ is set and vice versa.							
Bit 2	Receive Buffer Error Interrupt Status. This IRQ is triggered in one of two ways: (1) When the receive buffer is empty and there is an attempt to read data. (2) When the receive buffer is full and more data is received. This flag is cleared when RX GO is set and a SOP is received.							
Bit 1	Packet Receive Complete Interrupt Status. This IRQ is triggered when a packet has been received. If transaction mode is enabled, then this bit is not set until after transmission of the ACK. If transaction mode is not enabled then this bit is set as soon as a valid packet is received. This bit is cleared when this register is read. RXC IRQ and RXE IRQ flags may change value at different times in response to a single event. There are cases when this bit is not triggered when ACK EN = 1 and there is an error in reception. Therefore, firmware should examine RXC IRQ, RXE IRQ, and CRC 0 to determine receive status. If the first read of this register returns RXC IRQ = 1 and RXE IRQ = 0 then firmware must execute a second read to this register to determine if an error occurred by examining the status of RXE IRQ. If the first read of this register returns RXC IRQ = 1 and RXE IRQ = 1 then the firmware must not execute a second read to this register for a given transaction.							
Bit 0	Receive Error Interrupt Status. This IRQ is triggered when there is an error in reception. It is triggered whenever a packet is received with a bad CRC16, an unexpected EOP is detected, a packet type (data or ACK) mismatch, or a packet is dropped because the receive buffer is still not empty when the next packet starts. The exact cause of the error may be determined by reading RX_STATUS_ADR. This bit is cleared when this register is read.							

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## AWM24xxL Register Details

Mnemonic	RX_STATUS_ADR			Address				0x08
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	1	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode	

It is expected that firmware does not read this register until after TX GO self clears. Status bits are non-atomic (different flags may change value at different times in response to a single event).

- Bit 7 RX Packet Type. This bit is set when the received packet is an ACK packet, and cleared when the received packet is a standard packet.
- Bit 6 Receive Packet Type Error. This bit is set when the packet type received is what not was expected and cleared when the packet type received was as expected. For example, if a data packet is expected and an ACK is received, this bit will be set.
- Bit 5 Unexpected EOP. This bit is set when an EOP is detected before the expected data length and CRC16 fields have been received. This bit is cleared when SOP pattern for the next packet has been received. This includes the case where there are invalid bits detected in the length field and the length field is forced to 0.
- Bit 4 Zero-seed CRC16. This bit is set whenever the CRC16 of the last received packet has a zero seed.
- Bit 3 Bad CRC16. This bit is set when the CRC16 of the last received packet is incorrect.
- Bit 2 Receive Code Length. This bit indicates the DATA\_CODE\_ADR code length used in the last correctly received packet. 1 = 64-chip code, 0 = 32-chip code.
- Bits 1:0 Receive Data Mode. These bits indicate the data mode of the last correctly received packet. 00 = 1-Mbps GFSK 01 = 8DR 10 = DDR. 11 = Not Valid. These bits do not apply to unframed packets.

Mnemonic	RX_COUNT_ADR			Address				0x09
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Function	RX Count							

Count bits are non-atomic (updated at different times).

- Bits 7:0 This register contains the total number of payload bytes received during reception of the current packet. After packet reception is complete, this register will match the value in RX\_LENGTH\_ADR unless there was a packet error. This register is reset to 0x00 when RX\_LENGTH\_ADR is loaded. Count should not be read when RX\_GO=1 during a transaction.

Mnemonic	RX_LENGTH_ADR			Address				0x0A
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Function	RX Length							

Length bits are non-atomic (different flags may change value at different times in response to a single event).

- Bits 7:0 This register contains the length field which is updated with the reception of a new length field (shortly after start of packet detected). If there is an error in the received length field, 0x00 is loaded instead, except when using GFSK datarate, and an error is flagged.

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## AWM24xxL Register Details

Mnemonic	PWR_CTRL_ADR				Address			0x0B
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	-	0	0	0	0
Read/Write	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Function	PMU EN	LVIRQ EN	PMU SEN	Not Used	LVI TH		PMU OUTV	
Bit 7	Power Management Unit (PMU) Enable. Setting this bit enables the PMU. When the PMU is disabled, or if the PMU is enabled and the $V_{BAT}$ voltage is above the value set in Bits 1:0 of this register, the $V_{REG}$ pin is internally connected to the $V_{BAT}$ pin. if the PMU is enabled and the $V_{BAT}$ voltage is below the value set by PMU OUTV, then the PMU will boost the $V_{REG}$ pin to a voltage not less than the value set by PMUOP.							
Bit 6	Low Voltage Interrupt Enable. Setting this bit enables the LV IRQ interrupt. When this interrupt is enabled, if the $V_{BAT}$ voltage falls below the threshold set by LVI TH, then a low voltage interrupt will be generated. The LVI is not available when the device is in sleep mode. The LVI event on IRQ pin is automatically disabled whenever the PMU is disabled.							
Bit 5	PMU Sleep Mode Enable. If this bit is set, the PMU will continue to operate normally when the device is in sleep mode. If this bit is not set, then the PMU is disabled when the device is in sleep mode. In this case, if $V_{BAT}$ is below the PMU OUTV voltage and PMU EN is set, when the device enters sleep mode the $V_{REG}$ voltage falls to the $V_{BAT}$ voltage as the $V_{REG}$ capacitors discharge.							
Bits 3:2	Low Voltage Interrupt Threshold. This field sets the voltage on $V_{BAT}$ at which the LVI is triggered. 11 = 1.8V; 10 = 2.0V; 01 = 2.2V; 00 = PMU OUTV voltage.							
Bits 1:0	PMU Output Voltage. This field sets the minimum output voltage of the PMU. 11 = 2.4V; 10 = 2.5V; 01 = 2.6V; 00 = 2.7V. When the PMU is active, the voltage output by the PMU on $V_{REG}$ will never be less than this voltage provided that the total load on the $V_{REG}$ pin is less than the specified maximum value, and the voltage in $V_{BAT}$ is greater than the specified minimum value.							

Mnemonic	XTAL_CTRL_ADR			Address				0x0C
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	-	-	1	0	0
Read/Write	R/W	R/W	R/W	-	-	R/W	R/W	R/W
Function	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ		
Bits 7:6	XOUT Pin Function. This field selects between the different functions of the XOUT pin. 00 = Clock frequency set by XOUT FREQ; 01 = Active LOW PA Control; 10 = Radio data serial bit stream. If this option is selected and SPI is configured for 3-wire mode then the MISO pin will output a serial clock associated with this data stream; 11 = GPIO. To disable this output, set to GPIO mode, and set the GPIO state in IO_CFG_ADR.							
Bit 5	Crystal Stable Interrupt Enable. This bit enables the OS IRQ interrupt. When enabled, this interrupt generates an IRQ event when the crystal has stabilized after the device has woken from sleep mode. This event is cleared by writing zero to this bit.							
Bits 2:0	XOUT Frequency. This field sets the frequency output on the XOUT pin when XOUT FN is set to 00. 0 = 12 MHz; 1 = 6 MHz, 2 = 3 MHz, 3 = 1.5 MHz, 4 = 0.75 MHz; other values are not defined.							



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## AWM24xxL Register Details

Mnemonic	IO_CFG_ADR			Address				0x0D
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	IRQ OD	IRQ POL	MISO OD	XOUT OD	PACTL OD	PACTL GPIO	SPI 3PIN	IRQ GPIO
To use a GPIO pin as an input, the output mode must be set to open drain, and a "1" written to the corresponding output register bit.								
Bit 7	IRQ Pin Drive Strength. Setting this bit configures the IRQ pin as an open drain output. Clearing this bit configures the IRQ pin as a standard CMOS output, with the output "1" drive voltage being equal to the $V_{IO}$ pin voltage.							
Bit 6	IRQ Polarity. Setting this bit configures the IRQ signal polarity to be active HIGH. Clearing this bit configures the IRQ signal polarity to be active low.							
Bit 5	MISO Pin Drive Strength. Setting this bit configures the MISO pin as an open drain output. Clearing this bit configures the MISO pin as a standard CMOS output, with the output "1" drive voltage being equal to the $V_{IO}$ pin voltage.							
Bit 4	XOUT Pin Drive Strength. Setting this bit configures the XOUT pin as an open drain output. Clearing this bit configures the XOUT pin as a standard CMOS output, with the output "1" drive voltage being equal to the $V_{IO}$ pin voltage.							
Bit 3	PACTL Pin Drive Strength. Setting this bit configures the PACTL pin as an open drain output. Clearing this bit configures the PACTL pin as a standard CMOS output, with the output "1" drive voltage being equal to the $V_{IO}$ pin voltage.							
Bit 2	PACTL Pin Function. When this bit is set the PACTL pin is available for use as a GPIO.							
Bit 1	SPI Mode. When this bit is cleared, the SPI interface acts as a standard 4-wire SPI Slave interface. When this bit is set, the SPI interface operates in "3-Wire Mode" combining MISO and MOSI on the same pin (SDAT), and the MISO pin is available as a GPIO pin.							
Bit 0	IRQ Pin Function. When this bit is cleared, the IRQ pin is asserted when an IRQ is active; the polarity of this IRQ signal is configurable in IRQ POL. When this bit is set, the IRQ pin is available for use as a GPIO pin, and the IRQ function is multiplexed onto the MOSI pin. In this case the IRQ signal state is presented on the MOSI pin whenever the $\overline{SS}$ signal is inactive (HIGH).							

Mnemonic	GPIO_CTRL_ADR			Address				0x0E
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	-	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Function	XOUT OP	MISO OP	PACTL OP	IRQ OP	XOUT IP	MISO IP	PACTL IP	IRQ IP
To use a GPIO pin as an input, the output mode must be set to open drain, and a "1" written to the corresponding output register bit.								
Bit 7	XOUT Output. When the XOUT pin is configured to be a GPIO, the state of this bit sets the output state of the XOUT pin.							
Bit 6	MISO Output. When the MISO pin is configured to be a GPIO, the state of this bit sets the output state of the MISO pin.							
Bit 5	PACTL Output. When the PACTL pin is configured to be a GPIO, the state of this bit sets the output state of the PACTL pin.							
Bit 4	IRQ Output. When the IRQ pin is configured to be a GPIO, the state of this bit sets the output state of the IRQ pin.							
Bit 3	XOUT Input. When the XOUT pin is configured to be a GPIO, the state of this bit reflects the voltage on the XOUT pin.							
Bit 2	MISO Input. When the MISO pin is configured to be a GPIO, the state of this bit reflects the voltage on the MISO pin.							
Bit 1	PACTL Input. When the PACTL pin is configured to be a GPIO, the state of this bit reflects the voltage on the PACTL pin.							
Bit 0	IRQ Input. When the IRQ pin is configured to be a GPIO, the state of this bit reflects the voltage on the IRQ pin.							

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## AWM24xxL Register Details

Mnemonic	XACT_CFG_ADR			Address			0x0F	
Bit	7	6	5	4	3	2	1	0
Default	1	-	0	0	0	0	0	0
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Function	ACK EN	Not Used	FRC END	END STATE			ACK TO	
Bit 7	Acknowledge Enable. When this bit is set, an ACK packet is automatically transmitted whenever a valid packet is received; in this case the device is considered to be in transaction mode. After transmission of the ACK packet, the device automatically transitions to the END STATE. When this bit is cleared, the device transitions directly to the END STATE immediately after the end of packet transmission.							
Bit 5	Force End State. Setting this bit forces a transition to the state set in END STATE. By setting the desired END STATE at the same time as setting this bit the device may be forced to immediately transition from its current state to any other state. This bit is automatically cleared upon completion.							
Bits 4:2	Transaction End State. This field defines the mode to which the device transitions after receiving or transmitting a packet. 000 = Sleep Mode; 001 = Idle Mode; 010 = Synth Mode (TX); 011 = Synth Mode (RX); 100 = RX Mode. In normal use, this field will typically be set to 000 or 001 when the device is transmitting packets, and 100 when the device is receiving packets. Note that when the device transitions to receive mode as an END STATE, the receiver must still be armed by setting RX GO before the device can begin receiving data. If the system only support packets <=16 bytes then firmware should examine RXC IRQ and RXE IRQ to determine the status of the packet. If the system supports packets > 16 bytes ensure that END STATE is not sleep, force RXF=1, perform receive operation, force RXF=0, and if necessary set END STATE back to sleep.							
Bits 1:0	ACK Timeout. When the device is configured for transaction mode, this field sets the timeout period after transmission of a packet during which an ACK must be correctly received in order to prevent a transmit error condition from being detected. This timeout period is expressed in terms of a number of SOP_CODE_ADR code lengths; if SOP LEN is set, then the timeout period is this value multiplied by 64 μs and if SOP LEN is cleared then the timeout is this value multiplied by 32 μs. 00 = 4x; 01 = 8x, 10 = 12x; 11 = 15x the SOP_CODE_ADR code length. ACK_TO must be set to greater than 30 + Data Code Length (only for 8DR) + Preamble Length + SOP Code Length (x2).							

Mnemonic	FRAMING_CFG_ADR			Address				0x10
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	0	0	1	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	SOP EN	SOP LEN	LEN EN	SOP TH				
Bit 7	SOP Enable. When this bit is set, each transmitted packet begins with a SOP field, and only packets beginning with a valid SOP field will be received. If this bit is cleared, no SOP field will be generated when a packet is transmitted, and packet reception will begin whenever two successive correlations against the DATA_CODE_ADR code are detected.							
Bit 6	SOP PN Code Length. When this bit is set the SOP_CODE_ADR code length is 64 chips. When this bit is cleared the SOP_CODE_ADR code length is 32 chips.							
Bit 5	Packet Length Enable. When this bit is set the 8-bit value contained in TX_LENGTH_ADR is transmitted immediately after the SOP field. In receive mode, the 8 bits immediately following the SOP field are interpreted as the length of the packet. When this bit is cleared no packet length field is transmitted. 8DR always sends the packet length field (forces LEN EN =1). GFSK requires user set LEN EN = 1.							
Bits 4:0	SOP Correlator Threshold. This is the receive data correlator threshold used when attempting to detect a SOP symbol. There is a threshold for the SOP_CODE_ADR code. This (single) threshold is applied independently to each of SOP1 and SOP2 fields. There are then two thresholds for each of the 64-chip DATA_CODE_ADR codes and 32 chip DATA_CODE_ADR codes. When SOP LEN is set, all 5 bits of this field are used. When SOP LEN is cleared, the most significant bit is disregarded. Typical applications configure SOP TH = 04h for SOP32 and SOP TH = 0Eh for SOP64.							

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## AWM24xxL Register Details

Mnemonic	DATA32_THOLD_ADR			Address				0x11
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	0	1	0	0
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	Not Used	TH32			
Bits 3:0:	32 Chip Data PN Code Correlator Threshold. This register sets the correlator threshold used in DSSS modes when DATA CODE LENGTH (see TX_CFG_ADR) is set to 32. Typical applications configure TH32 = 05h.							

Mnemonic	DATA64_THOLD_ADR			Address				0x12
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	0	1	0	1	0
Read/Write	-	-	-	R/W	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	TH64				
Bits 4:0	64 Chip Data PN Code Correlator Threshold. This register sets the correlator threshold used in DSSS modes when the DATA CODE LENGTH (see TX_CFG_ADR) is set to 64. Typical applications configure TH64 = 0Eh.							

Mnemonic	RSSI_ADR			Address				0x13
Bit	7	6	5	4	3	2	1	0
Default	0	-	1	0	0	0	0	0
Read/Write	R	-	R	R	R	R	R	R
Function	SOP	Not Used	LNA	RSSI				
A Received Signal Strength Indicator (RSSI) reading is taken automatically when an SOP symbol is detected. In addition, an RSSI reading is taken whenever RSSI_ADR is read. The contents of this register are not valid after the device is configured for receive mode until either a SOP symbol is detected, or the register is read. The conversion can occur as often as once every 12-μs.								
If it is desired to measure the background RF signal strength on a channel before a packet has been received then the MCU should perform a “dummy” read of this register, the results of which should be discarded. This “dummy” read will cause an RSSI measurement to be taken, and therefore subsequent readings of the register will yield valid data.								
Bit 7	SOP RSSI Reading. When set, this bit indicates that the reading in the RSSI field was taken when a SOP symbol was detected. When cleared, this bit indicates that the reading stored in the RSSI field was triggered by a previous SPI read of this register.							
Bit 5	LNA State. This bit indicates the LNA state when the RSSI reading was taken. When cleared, this bit indicates that the LNA was disabled when the RSSI reading was taken; if set this bit indicates that the LNA was enabled when the RSSI reading was taken.							
Bits 4:0	RSSI Reading. This field indicates the instantaneous strength of the RF signal being received at the time that the RSSI reading was taken. A larger value indicates a stronger signal. The signal strength measured is for the RF signal on the configured channel, and is measured after the LNA stage.							

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## AWM24xxL Register Details

Mnemonic	EOP_CTRL_ADR			Address				0x14
Bit	7	6	5	4	3	2	1	0
Default	1	0	1	0	0	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	HEN	HINT			EOP			
If the LEN EN bit is set, then the contents of this register have no effect. If the LEN EN bit is cleared, then this register is used to configure how an EOP (end of packet) condition is detected.								
Bit 7	EOP Hint Enable. When set, this bit will cause an EOP to be detected if no correlations have been detected for the number of symbol periods set by the HINT field and the last two received bytes match the calculated CRC16 for all previously received bytes. Use of this mode reduces the chance of non-correlations in the middle of a packet from being detected as an EOP condition.							
Bits 6:4	EOP Hint Symbol Count. The minimum number of symbols of consecutive non-correlations at which the last two bytes are checked against the calculated CRC16 to detect an EOP condition.							
Bits 4:0	EOP Symbol Count. An EOP condition is deemed to exist when the number of consecutive non-correlations is detected.							

Mnemonic	CRC_SEED_LSB_ADR			Address				0x15
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CRC SEED LSB							
The CRC16 seed allows different devices to generate or recognize different CRC16s for the same payload data. If a transmitter and receiver use a randomly selected CRC16 seed, the probability of correctly receiving data intended for a different receiver is 1/65535, even if the other transmitter/receiver are using the same SOP_CODE_ADR codes and channel.								
Bits 7:0      CRC16 Seed Least Significant Byte. The LSB of the starting value of the CRC16 calculation.								

Mnemonic	CRC_SEED_MSB_ADR			Address				0x16
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CRC SEED MSB							
Bits 7:0	CRC16 Seed Most Significant Byte. The MSB of the starting value of the CRC16 calculation.							

Mnemonic	TX_CRC_LSB_ADR			Address				0x17
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	TX CRC LSB							
Bits 7:0	Calculated CRC16 LSB. The LSB of the CRC16 that was calculated for the last transmitted packet. This value is only valid after packet transmission is complete.							

Mnemonic	TX_CRC_MSB_ADR			Address				0x18
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Function	TX CRC MSB							
Bits 7:0	Calculated CRC16 MSB. The MSB of the CRC16 that was calculated for the last transmitted packet. This value is only valid after packet transmission is complete.							

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## AWM24xxL Register Details

Mnemonic	RX_CRC_LSB_ADR			Address				0x19
Bit	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1
Read/Write	R	R	R	R	R	R	R	R
Function	RX CRC LSB							
Bits 7:0	Received CRC16 LSB. The LSB of the CRC16 field from the last received packet. This value is valid whether or not the CRC16 field matched the calculated CRC16 of the received packet.							

Mnemonic	RX_CRC_MSB_ADR			Address				0x1A
Bit	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1
Read/Write	R	R	R	R	R	R	R	R
Function	RX CRC MSB							
Bits 7:0	Received CRC16 MSB. The MSB of the CRC16 field from the last received packet. This value is valid whether or not the CRC16 field matched the calculated CRC16 of the received packet.							

Mnemonic	TX_OFFSET_LSB_ADR			Address				0x1B
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R	R	R	R	R	R	R
Function	STRIM LSB							
Bits 7:0	<p>The least significant 8 bits of the synthesizer offset value. This is a 12-bit 2's complement signed number which may be used to offset the transmit frequency of the device by up to <math>\pm 1.5</math> MHz. A positive value increases the transmit frequency, and a negative value reduces the transmit frequency. A value of +1 increases the transmit frequency by 732.6 Hz; a value of -1 decreases the transmit frequency by 732.6 Hz. A value of 0x0555 increases the transmit frequency by 1 MHz; a value of 0xAAB decreases the transmit frequency by 1 MHz. Typically, this register is loaded with 0x55 during initialization. Typically this feature is used to avoid the need to change the synthesizer frequency when switching between TX and RX. As the IF = 1 MHz the RX frequency is offset 1 MHz from the synthesizer frequency; therefore, transmitting with a 1 MHz offset allows the same synthesizer frequency to be used for both transmit and receive.</p> <p>Synthesizer offset has no effect on receive frequency.</p>							

Mnemonic	TX_OFFSET_MSB_ADR			Address				0x1C
Bit	7	6	5	4	3	2	1	0
Default	-	-	-	-	0	0	0	0
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Function	Not Used	Not Used	Not Used	Not Used	STRIM MSB			
Bits 3:0      The most significant 4 bits of the synthesizer trim value. Typically, this register is loaded with 0x05 during initialization.								

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## AWM24xxL Register Details

Mnemonic	MODE_OVERRIDE_ADR			Address				0x1D
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	-	-	0
Read/Write	W	W	W	W	W	-	-	W
Function	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST

Bits 7	Reserved. Do not write a 1 to these bits.
Bits 5	Manually Initiate Synthesizer. Setting this bit forces the synthesizer to start. Clearing this bit has no effect. For this bit to operate correctly, the oscillator must be running before this bit is set.
Bits 4:3	Force Awake. Force the device out of sleep mode. Setting both bits of this field forces the oscillator to keep running at all times regardless of the END STATE setting. Clearing both of these bits disables this function.
Bits 0	Reset. Setting this bit forces a full reset of the device. Clearing this bit has no effect.

Mnemonic	RX_OVERRIDE_ADR			Address				0x1E
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Function	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used

This register provides the ability to over-ride some automatic features of the device.	
Bits 7	When this bit is set, the device uses the transmit synthesizer frequency rather than the receive synthesizer frequency for the given channel when automatically entering receive mode.
Bits 6	When this bit is set and ACK EN is enabled, the transmission of the ACK packet is delayed by 20 $\mu$ s.
Bits 5	Force Expected Packet Type. When this bit is set, and the device is in receive mode, the device is configured to receive an ACK packet at the data rate defined in TX_CFG_ADR.
Bits 4	Force Receive Data Rate. When this bit is set, the receiver will ignore the data rate encoded in the SOP symbol, and will receive data at the data rate defined in TX_CFG_ADR.
Bits 3	Reject packets with a zero-seed CRC16. Setting this bit causes the receiver to reject packets with a zero-seed, and accept only packets with a CRC16 that matches the seed in CRC_SEED_LSB_ADR and CRC_SEED_MSB_ADR.
Bits 2	The RX CRC16 checker is disabled. If packets with CRC16 enabled are received, the CRC16 will be treated as payload data and stored in the receive buffer.
Bits 1	Accept Bad CRC16. Setting this bit causes the receiver to accept packets with a CRC16 that do not match the seed in CRC_SEED_LSB_ADR and CRC_SEED_MSB_ADR. An ACK is to be sent regardless of the condition of the received CRC16.

Mnemonic	TX_OVERRIDE_ADR			Address				0x1F
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV

This register provides the ability to over-ride some automatic features of the device.	
Bits 7	When this bit is set, the device uses the receive synthesizer frequency rather than the transmit synthesizer frequency for the given channel when automatically entering transmit mode.
Bits 6	Force Preamble. When this bit is set, the device will transmit a continuous repetition of the preamble pattern (see PREAMBLE_ADR) after TX GO is set. This mode is useful for some regulatory approval procedures.
Bits 5	Reserved. Do not write a 1 to this bit.
Bits 4	Transmit ACK Packet. When this bit is set, the device sends an ACK packet when TX GO is set.
Bits 3	ACK Override. Use TX_CFG_ADR to determine the data rate and the CRC16 used when transmitting an ACK packet.
Bits 2	Disable Transmit CRC16. When set, no CRC16 field is present at the end of transmitted packets.
Bits 1	Reserved. Do not write a 1 to this bit.
Bits 0	TX Data Invert. When this bit is set the transmit bitstream is inverted.

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## AWM24xxL Register Details

Mnemonic	CLK_OFFSET_ADR			Address				0x27
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:2      Reserved. Do not write a 1 to these bits.								
Bits 1        Force Receive Clock								
Bits 0        Reserved. Do not write a 1 to this bit.								

Mnemonic	CLK_EN_ADR			Address				0x28
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:2      Reserved. Do not write a 1 to these bits.								
Bits 1        Force Receive Clock Enable. Typical application will set this bit during initialization.								
Bits 0        Reserved. Do not write a 1 to this bit.								

Mnemonic	RX_ABORT_ADR			Address				0x29
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:6      Reserved. Do not write a 1 to these bits.								
Bits 5        Receive Abort Enable.								
Bits 4:0      Reserved. Do not write a 1 to these bits.								

Mnemonic	AUTO_CAL_TIME_ADR			Address				0x32
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	1	1
Read/Write	W	W	W	W	W	W	W	W
Function	AUTO_CAL_TIME_MAX							
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:0      Auto Cal Time Max. Firmware must write 3Ch to this register during initialization.								

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## AWM24xxL Register Details

Mnemonic	AUTO_CAL_OFFSET_ADR			Address				0x35
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	AUTO_CAL_OFFSET_MINUS_4							
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:0      Auto Cal Time Max. Firmware must write 14h to this register during initialization.								

Mnemonic	ANALOG_CTRL_ADR			Address				0x39
Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W
Function	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ALL SLOW
This register provides the ability to over-ride some automatic features of the device.								
Bits 7:1      Reserved. Do not write a 1 to these bits.								
Bits 0      All Slow. When set, the synth settling time for all channels is the same as for slow channels. It is recommended that firmware set this bit when using GFSK data rate mode.								



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## AWM24xxL Register Details

### 9.1 Register Files

Files are written to or read from using non-incrementing burst read or write transactions. In most cases reading a file may be destructive; the file must be completely read, otherwise the contents may be altered.

Mnemonic	TX_BUFFER_ADR	Address	0x20
Length	16 Bytes	R/W	W
Default	0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF		

The transmit buffer is a FIFO. Writing to this file adds a byte to the packet being sent. Writing more bytes to this file than the packet length in TX\_LENGTH\_ADR will have no effect, and these bytes will be lost after successful packet transmission. It is **NOT** possible to load two-eight byte packets into this register, and then transmit them sequentially by enabling the TX GO bit twice; this would have the effect of sending the first eight bytes twice.

Mnemonic	RX_BUFFER_ADR	Address	0x21
Length	16 Bytes	R/W	R
Default	0xFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF		

The receive buffer is a FIFO. Received bytes may be read from this file register at any time that it is not empty, but when reading from this file register before a packet has been completely received care must be taken to ensure that error packets (for example with bad CRC16) are handled correctly.

When the receive buffer is configured to be overwritten by new packets (the alternative is for new packets to be discarded if the receive buffer is not empty), similar care must be taken to verify after the packet has been read from the buffer that no part of it was overwritten by a newly received packet while this file register is being read.

When the VLD EN bit in RX\_CFG\_ADR is set, the bytes in this file register alternate—the first byte read is data, the second byte is a valid flags for each bit in the first byte, the third byte is data, the fourth byte valid flags, etc. In SDR and DDR modes the valid flag for a bit is set if the correlation coefficient for the bit exceeded the correlator threshold, and is cleared if it did not. In 8DR mode, the MSB of a valid flags byte indicates whether or not the correlation coefficient of the corresponding received symbol exceeded the threshold. The seven LSBs contain the number of erroneous chips received for the data.

Mnemonic	SOP_CODE_ADR	Address	0x22
Length	8 Bytes	R/W	R/W
Default	0x17FF9E213690C782		

When using 32 chip SOP\_CODE\_ADR codes, only the first four bytes of this register are used; in order to complete the file write process, these four bytes must be followed by four bytes of “dummy” data. However, a class of codes known as “multiplicative codes” may be used; there are 64 chip codes with good auto-correlation and cross-correlation properties where the least significant 32 chips themselves have good auto-correlation and cross-correlation properties when used as 32-chip codes. In this case the same eight-byte value may be loaded into this file and used for both 32 chip and 64 chip SOP symbols.

When reading this file, all eight bytes must be read; if fewer than eight bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.

Recommended SOP Codes:

```

0x91CCF8E291CC373C
0x0FA239AD0FA1C59B
0x2AB18FD22AB064EF
0x507C26DD507CCD66
0x44F616AD44F6E15C
0x46AE31B646AECC5A
0x3CDC829E3CDC78A1
0x7418656F74198EB9
0x49C1DF6249C0B1DF
0x72141A7F7214E597

```

# ARTAFLEX

## AWM24xxL Register Details

Mnemonic	DATA_CODE_ADR	Address	0x23
Length	16 Bytes	R/W	R/W
Default	0x02F9939702FA5CE3012BF1DB0132BE6F		
<p>This file is ignored when using the device in 1-Mbps GFSK mode. In 64-SDR mode, only the first eight bytes are used; in order to complete the file write process, these eight bytes must be followed by eight bytes of "dummy" data. In 32-SDR mode, only four bytes are used, and in 32-DDR mode only eight bytes are used. In 64-DDR and 8DR modes, all sixteen bytes are used. Certain sixteen-byte sequences have been calculated that provide excellent auto-correlation and cross-correlation properties, and it is recommended that such sequences be used; the default value of this register is one such sequence. In typical applications, all devices use the same DATA_CODE_ADR codes, and devices and systems are addressed by using different SOP_CODE_ADR codes; in such cases it may never be necessary to change the contents of this register from the default value.</p> <p>When reading this file, all sixteen bytes must be read; if fewer than sixteen bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.</p> <p>Typical applications should use the default code.</p>			

Mnemonic	PREAMBLE_ADR	Address	0x24
Length	3 Bytes	R/W	R/W
Default	0x333302		
<p>1st byte – The number of repetitions of the preamble sequence that are to be transmitted. The preamble may be disabled by writing 0x00 to this byte.</p> <p>2nd byte – Least significant eight chips of the preamble sequence</p> <p>3rd byte – Most significant eight chips of the preamble sequence</p> <p>If using 64-SDR to communicate with CYWUSB69xx devices, set number of repetitions to four for optimum performance</p> <p>When reading this file, all three bytes must be read; if fewer than three bytes are read from the file, the contents of the file will have been rotated by the number of bytes read. This applies to writes, as well.</p>			

Mnemonic	MFG_ID_ADR	Address	0x25
Length	6 Bytes	R	R
Default	NA		
<p>1st byte – 4 bits version + 2 bits vendor ID + high 2 bits of Year</p> <p>2nd through 6th bytes: Manufacturing ID for the device.</p> <p>To minimize ~190µA of current consumption (default), execute a "dummy" single-byte SPI write to this address with a zero data stage after the contents have been read. Non-zero to enable reading of fuses. Zero to disable reading fuses.</p>			